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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,241	12/31/2003	Jeong Ho Park	09407.0001	6968

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 10/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/748,241	PARK, JEONG HO
	Examiner	Art Unit
	Stanetta D. Isaac	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-23* is/are allowed.

6)☒ Claim(s) *1-12 and 24-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment filed on 7/11/05. Currently, claims 1-31 are pending.

Drawings

The drawings were received on 7/11/05. These replacement drawings are in response to the objection to the drawings in the Office Action mailed on 3/10/05. The Examiner has reviewed the corrected replacement drawings and has now withdrawn the objection to the drawings.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7, 9 and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Gardner et al., US Patent 5,780,340.

Gardner discloses the semiconductor method as claimed. See figures 1A-1Q, and corresponding text, where Gardner teaches, pertaining to claim 1, a method for fabricating a semiconductor transistor, comprising: forming a first insulating layer **106** on a semiconductor substrate **102** (figure1B; col. 3, lines 65-67; col. 4, lines 1-4); forming an LDD region **162A/162B** using ion implantation (figures 1O and 1P; col. 6, lines 61-67; col. 7, lines 1-45);

patterning the first insulating layer (figure 1C-1D; col. 4, lines 5-41); forming a trench **112/114** in the substrate (figures 1C and 1D; col. 4, lines 5-41); forming a trench gate **142** by depositing and planarizing a second insulating layer **130A/130B/132A/132B** and a conductor on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor (figures 1H and 1I; col. 5, lines 58-67; col. 6, lines 1-14); forming a photoresist pattern **152** on the substrate (figures 1M and 1N; col. 6, lines 42-60); forming source/drain regions **160A/160B** by performing an ion implantation using the photoresist pattern as a mask (figures 1O and 1P; col. 6, lines 61-67; col. 7, lines 1-54); and removing the photoresist pattern and the first insulating layer **106** (figures 1N and 1P; col. 6, lines 49-60; col. col. 7, lines 33-35 ***Note***: Gardner teaches partially removing the first insulating layer).

Pertaining to claim 2, Gardner teaches, the method further comprising performing a thermal process after removing the first insulating layer (col. 7, lines 33-36).

Pertaining to claim 3, Gardner teaches, the method wherein the first insulating layer works as a buffer layer during the ion implantation for forming the LDD and the source/drain regions (col. 7, lines 19-37 ***Note***: since Gardner teaches that the lower oxide spacer portions blocks a substantial amount of ions to form the LDD regions and allows a substantial amount of ions to pass through the substrate to form the source drain regions, it is inherent that the first insulating layer is used as a buffer layer)

Pertaining to claim 4, Gardner teaches the method wherein the first insulating layer is made of one selected from the group consisting of nitrides, tantalum oxides, titanium oxides, and hafnium oxides (col. 3, lines 65-67, silicon dioxide).

Pertaining to claim 5, Gardner teaches the method wherein the conductor is made of one selected form the group consisting of tungsten alloys, titanium alloys, and tantalum alloys (col. 8, lines 49-51).

Pertaining to claim 6, Gardner teaches the method wherein the energy of the ion implantation for forming the LDD region is between 30keV and 80keV (col. 6, lines 61-64).

Pertaining to claim 7, Gardner teaches the method wherein the energy of the ion implantation for forming the source/drain regions is between 5keV and 60keV (col. 6, lines 61-64).

Pertaining to claim 9, Gardner teaches the method wherein the trench is formed using chemical dry etching (figure 1D; col. 4, lines 23-26).

Pertaining to claim 11, Gardner teaches the method wherein planarizing the second insulating layer and the conductor comprises a CMP process using the first insulating layer as an etch-stop layer (figure 1I; col. 5, lines 58-67).

Pertaining to claim 12, Gardner teaches the method wherein the first insulating layer is removed by a wet etching using a phosphoric acid solution (figure 1N; col. 6, lines 49-60; col. 8, lines 53-55).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 24-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Sugawara et al., US Patent 6,171,916.

Sugawara discloses the semiconductor method as claimed. See figures 1A-2L, with emphasis on figures 2A-2L, and corresponding text, where Sugawara teaches, pertaining to claim 24, a method for fabricating a semiconductor transistor comprising: depositing a first insulating layer **5** on a semiconductor substrate **1**(figure 2D; col. 4. lines 20-24; col. 7, lines 34-40); forming an LDD region **7** using an ion implantation (figures 2G and 2L; col. 52-67); patterning the first insulating layer **5** (figure 2D; col. 7, lines 21-29); forming a trench **6** in the substrate (figure 2D; col. 7, lines 25-29); forming a trench gate **22** by depositing and planarizing a second insulating layer **21/23** and a first conductor **11** on the substrate with the trench (figure 2H; col. 8, lines 4-24, ***Note***: the Examiner takes the position than a planarizing process is achieved since the oxidized film is removed by a wet etching technique and that is appears that the surface is flat); depositing a second conductor **24** on the substrate with the trench gate formed thereon (figure 2I; col. 8, lines 22-31); patterning the second conductor and the first insulating layer (figures 2H-2J; col. 8, lines 1-46 ***Note***: the part of the second insulating layer is removed as stated in col. 8, lines 22-24); and forming source/drain regions **12** by performing an ion implantation using the patterned second conductor as a mask (col. 8, lines 60-64 ***Note***: Sugawara teaches that the ion implantation can be performed after the formation of the salicide structure).

Pertaining to claim 25, Sugawara teaches the method wherein the first insulating layer works as a buffer layer during the ion implantation for forming the LDD region (figure 2G; col. 7, lines 52-67 ***Note***: Sugawara teaches the impurities are diffused through the silicon nitride layer (first insulating layer)).

Pertaining to claim 26, Sugawara teaches the method wherein the first insulating layer is a nitride layer (col. 7, lines 43-46)

Pertaining to claim 27, Sugawara fails to show, the method wherein the first conductor is made of polysilicon and the second conductor is made of on selected from the group consisting of tungsten alloys, titanium alloys, and tantalum alloys (col. 7, lines 40-42).

Pertaining to claim 28, Sugawara s the method wherein the energy of the ion implantation for forming the LDD region is between 5keV and 60keV (col. 4 , lines 48-54).

Pertaining to claim 29, Sugawara teaches the method wherein the energy of the ion implantation for forming the source/drain regions is between 30keV and 80keV (col. 5, lines 35-39).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al., US Patent 5,780,340 in view of *Stanley Wolf and Richard N. Tauber, Silicon Processing for the VLSI Era, Vol. I, Lattice Press, 1986, pages 551-555.*

Gardner discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1-7, 9 and 11-12 under 35 U.S.C. 102(b).

However, Gardner fails to show, pertaining to claim 8, wherein the trench is formed by a dry etching with an etching angle between 5° and 30°. In addition, Gardner fails to show,

pertaining to claim 10, the method wherein lower edges of the trench are formed in a round shape.

Wolf teaches, on pages 551-555, a conventional method of using dry etching techniques for VLSI fabrication of semiconductor devices.

It would have been obvious to one of ordinary skill in the art to incorporate, the method wherein the trench is formed by a dry etching with an etching angle between 5° and 30°; the method wherein lower edges of the trench are formed in a round shape, in the method of Gardner, pertaining to claims 8 and 10, according to the conventional teachings of Wolf, with the motivation that, anisotropic dry etching is attractive in achieving a desired wall profile, where one of ordinary skill it the art would be drawn to the use of a directional dry etching method for the purpose of creating a desired trench wall profile.

Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugawara et al., US Patent 6,171,916.

Sugawara discloses the semiconductor method substantially as claimed. See preceding rejection of claims 24-29 under 35 U.S.C. 102(b). In addition, Sugawara shows, pertaining to claim 31, the method wherein the CMP process uses the first insulating layer as an etch-stop layer (col. 7, lines 43-51)

However, Sugawara fails to show, pertaining to claim 30, wherein planarizing a second insulating layer and a first conductor comprises a CMP process (col. 7, lines 43-51).

Sugawara teaches, in figure 2H, and corresponding text, where a polishing method may include reactive ion etching, wet etching technique or the use of both CMP and wet etching (col. 7, lines 43-51; col. 8, lines 4-24, the surface is wet etched).

Therefore it would have been obvious to one of ordinary skill in the art to substitute, wherein planarizing a second insulating layer and a first conductive comprises a CMP process, in the method of Sugawara, according to the teachings of Sugawara, with the motivation that, Sugawara teaches a planarized surface is shown in figure 2H, where the oxidized film is removed by a wet etching technique. Therefore, it would prove to be equivalent to use a CMP process instead since the ultimate goal is to create a planarized surface over the entire substrate including the second insulating layer and first conductor.

Response to Arguments

Applicant's arguments filed 7/11/05 have been fully considered but they are not persuasive. In the Remarks on pages 10-14:

The Applicant raises the clear issue as to whether Gardener, alone or in combination of Gardner in view of Wolf, or Sugawara, teaches or suggests the trench gate comprising the second insulating layer and the conductor.

The Examiner takes the position that Gardner, alone or in combination of Gardner in view of Wolf, and Sugawara does suggests the trench gate comprising the second insulating layer and the conductor. Specifically, as shown in figures 1H-1I, col. 5, lines 58-67; col. 6, lines 1-14, the second insulating layer **130A/130B/132A/132B** and conductor **142** is taught by Gardner. In addition, as shown in figure 2H; col. 8, lines 4-24, the second insulating layer **21**

and conductor **22** is taught by Sugawara. Furthermore, since Sugawara teaches that after the thermal oxidation process the oxidized film is removed by wet etching, the planarizing step is achieve.

Allowable Subject Matter

Claims 13-23 are allowed over the prior art of record, subjected to updated search.

The following is an examiner's statement of reasons for allowance:

The closest prior art of record, Gardner et al. US Patent 5,780,340, Gardner in view of Wolf, or Sugawara et al., US Patent 6,171,916, fails to show, the step of:

Pertaining to claim 13, "anisotropically etching the first insulating layer to form spacers;"

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

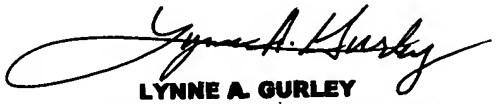
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Stanetta Isaac
Patent Examiner
September 26, 2005